Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): An apparatus comprising:

means for storing 2^{n-1} branch metric values to be used in a 1/n rate signal decoder to a storage device;

means for loading from the storage device no more than the 2^{n-1} branch metric values to generate 2^{K-1} signal states for each of an n-bit signal value received by a communications signal decoder, wherein K is a constraint length corresponding to a number of decoder state variables corresponding to the n-bits;

means for performing 2^{K-2} add, compare, select (ACS) butterfly calculations corresponding to the no more than 2^{n-1} branch metric values, including means for evaluating two path metrics in parallel responsive to a single vector add-subtract instruction to operate on two prior path metrics and stored branch metrics, and a single VITMAX instruction to compare the upper and lower bit values of two registers and store the two larger values in a third register.

Claim 2 (cancel)

Claim 3 (currently amended): The apparatus of claim [[2]] 1 wherein the means for performing 2^{K-2} ACS butterfly calculations comprises digital signal processor (DSP) registers and accumulators being used in 16-bit computation mode.

Claims 4 – 6 (cancel)

Claim 7 (currently amended): The apparatus of claim [[6]] 1 wherein the single VITMAX instruction is to store two decision bits into an accumulator in order to allow a selected path metric to be tracked.

Claim 8 (original): The apparatus of claim 7 wherein the 2^{K-2} ACS butterfly calculations are to be performed within two DSP processing cycles.

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Claim 9 (currently amended):   A method to perform a Viterbi decoding algorithm comprising:

initializing path metric buffers and trace back buffers;

evaluating branch metric (BM) kernel equations;

storing the result of the BM evaluations;

performing path metric evaluations corresponding to each BM evaluation, the path metric evaluations using a single vector add-subtract instruction to operate on two prior path metrics and two stored BMs and a single vector compare-select instruction to compare upper and lower portions of first and second register values, respectively, and to store the larger of the respective upper and lower portions in a third register and store two decision bits into an accumulator.

Claim 10 (original):   The method of claim 9 wherein the Viterbi decoding algorithm is to be performed by a 16-state, 1/3 rate decoder.

Claim 11 (original):   The method of claim 9 further comprising performing add, compare, and select (ACS) calculations to determine a most probable next state transition for each current state of an input signal to the Viterbi decoding algorithm.

Claim 12 (original):   The method of claim 11 further comprising determining a maximum path metric values corresponding to the path metric evaluations and storing them.

Claim 13 (original):   The method of claim 12 further comprising tracing back through state transitions to determine the minimum path between each bit state decoded by the Viterbi decoding algorithm.

Claim 14 (original):   The method of claim 9 wherein the number of BM equations is no more than 4.

Claim 15 (original):   The method of claim 11 wherein the ACS calculations comprise the BM calculations and path metric calculations for each current state.

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Claim 16 (original):   The method of claim 11 wherein the ACS calculations comprise path metric calculations and not BM calculations for each current state.

Claim 17 (original):   The method of claim 15 wherein the number of BM and path metric calculations are reduced by taking advantage of symmetry among a table of possible next state transitions corresponding to a received encoded signal.

Claim 18 (currently amended):   A processor comprising:

a storage unit to store 2^{n-1} branch metric values to be used in a 1/n rate signal decoder to a storage device;

a loading unit to load from the storage device no more than the 2^{n-1} branch metric values to generate 2^{K-1} signal states for each of an n-bit signal value received by a communications signal decoder, where K is a constraint length corresponding to a number of decoder state variables corresponding to the n-bits;

add, compare, and select (ACS) logic to perform 2^{K-2} ACS butterfly calculations corresponding to the no more than 2^{n-1} branch metric values, including path metric logic to evaluate and select two path metrics in parallel responsive to a single vector ACS instruction to operation on two prior path metrics and two stored branch metrics and a single vector compare-selection instruction to select the two path metrics.

Claim 19 (original):   The processor claim 18 wherein the storage unit is at least one memory location and the loading unit is a memory interface unit.

Claim 20 (cancel)

Claim 21 (currently amended):   The processor of claim [[20]] 18 wherein the ACS logic comprises digital signal processor (DSP) registers and accumulators to be used in 16-bit computation mode.

Claim 22 (cancel)

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Claim 23 (currently amended): The processor of claim [[22]] 18 wherein the path metric logic is to perform a VITMAX instruction to compare the upper and lower 16-bit values of two 32-bit DSP registers and store the larger ~~of the~~ two in a third register.

Claim 24 (original): The processor of claim 23 wherein the VITMAX instruction is to store two decision bits into an accumulator in order to allow a selected path metric to be tracked.

Claim 25 (original): The processor of claim 24 wherein the 2^{K-2} ACS butterfly calculations are to be performed within two DSP processing cycles.

Claim 26 (currently amended): A machine-readable medium having stored thereon a set of instructions, which if executed by a machine, cause the machine to perform a method comprising:
initializing path metric buffers and trace back buffers;
evaluating no more than 4 branch metric (BM) kernel equations;
storing the result of the BM evaluations;
evaluating path metric calculations corresponding to each BM evaluation, the path metric evaluations using a single vector add-subtract instruction to operate on two prior path metrics and two stored BMs and a single vector compare-select instruction to compare upper and lower portions of first and second register values, respectively, and to store the larger of the respective upper and lower portions in a third register and store two decision bits into an accumulator.

Claim 27 (original): The machine-readable medium of claim 26 further comprising instructions to determine the maximum path metric values corresponding to the path metric evaluation and store them.

Claim 28 (currently amended): The machine-readable medium of claim 27 further comprising instructions to trace back through state transitions to determine a minimum path between each bit state decoded by ~~the~~ a Viterbi decoding algorithm.

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Claim 29 (original):   The machine-readable medium of claim 28 further comprising instructions to reduce the number of BM and path metric calculations by taking advantage of symmetry among a table of possible next state transitions corresponding to a received encoded signal.

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